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6 the output driver circuitry outputs a first portion of
7 data in response to a rising edge transition of an
8 external clock signal; and

9 the output driver circuitry outputs a second portion
10 of data in response to a falling edge transition of the
11 external clock signal; and

12 a second integrated circuit device coupled to the external
13 signal line, the second integrated circuit device including:

14 output driver circuitry to output data onto the external
15 signal line wherein:

16 the output driver circuitry outputs a first portion of
17 data in response to a rising edge transition of the
18 external clock signal; and

19 the output driver circuitry outputs a second portion
20 of data in response to a falling edge transition of the
21 external clock signal.

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3
1. ~~153~~. The system of claim ~~151~~¹ wherein the first and second
2 integrated circuit devices each include a clock alignment circuit
3 coupled to the output driver circuitry.

4
1. ~~154~~. The system of claim ~~153~~³ wherein each clock alignment
2 circuit is a delay lock loop circuit to generate an internal clock
3 signal, and wherein the output driver circuitry outputs data in
4 response to the internal clock signal.

5
1. ~~155~~. The system of claim ~~151~~¹ wherein the first and second
integrated circuit devices each further include:

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multiplexer circuitry coupled to the output driver circuitry,
wherein:

in response to a first transition of the external clock
signal, the multiplexer circuitry couples the first portion of
data to an input of the output driver circuitry; and

in response to a second transition of the external clock
signal, the multiplexer circuitry couples the second portion
of data to the input of the output driver circuitry.

6
1. ~~156~~. The system of claim ~~155~~⁵ wherein the first and second
2 integrated circuit devices each further include a clock alignment
3 circuit to generate a first internal clock signal, and wherein the
4 multiplexer circuitry couples the first portion of data to the

A

5 input of the output driver circuitry in response to the first
6 internal clock signal.

1 ⁷
~~157~~. The system of claim ⁶~~156~~ wherein the clock alignment
2 circuit generates a second internal clock signal, and wherein the
3 multiplexer circuitry couples the second portion of data to the
4 input of the output driver circuitry in response to the second
5 internal clock signal.

1 ⁸
~~158~~. The system of claim ¹~~157~~ wherein both the rising edge
transition of the external clock signal and the falling edge
transition of the external clock signal transpire during a first
clock cycle of the external clock signal.

1 ⁹
~~159~~. The system of claim ¹~~157~~ wherein both the rising and
2 falling edge transitions of the external clock signal each include
3 a voltage swing of less than one volt.

1 ¹⁰
~~160~~. The system of claim ¹~~157~~ wherein the first and second
2 integrated circuit devices each further include:
3 input receiver circuitry to sample data from the external
4 signal line wherein:

5 the input receiver circuitry samples a first portion
6 of data in response to a rising edge transition of the
7 external clock signal; and

8 the input receiver circuitry samples a second portion
9 of data in response to a falling edge transition of the
10 external clock signal.

11
1 ~~161.~~ A system comprising:

2 a first integrated circuit device coupled to an external
3 signal line, the first integrated circuit device including:

4 output driver circuitry to output data onto the external
5 signal line wherein:
6
7

8 the output driver circuitry outputs a first portion of
9 data synchronously with respect to a rising edge transition
10 of an external clock signal; and
11

12 the output driver circuitry outputs a second portion of
13 data synchronously with respect to a falling edge transition
14 of the external clock signal; and
15

16 a second integrated circuit device coupled to the external
17 signal line, the second integrated circuit device including:

18 input receiver circuitry to sample data from the external
19 signal line wherein:
20

16 the input receiver circuitry samples the first portion
17 of data synchronously with respect to the rising edge
18 transition of the external clock signal; and
19 the input receiver circuitry samples the second
20 portion of data synchronously with respect to the falling
21 edge transition of the external clock signal.

12
1 162. The system of claim 11 further including a clock
2 generator coupled to a second external signal line to generate the
3 external clock signal, wherein the first and second integrated
4 circuit devices receive the external clock signal.

13
1 163. The system of claim 11 wherein the first integrated
2 circuit device further includes a clock alignment circuit to
3 receive the external clock signal and to generate an internal clock
4 signal, wherein the output driver circuitry outputs data in
5 response to the internal clock signal.

14
1 164. The system of claim 11 wherein the first integrated
2 circuit device further includes:
3 multiplexer circuitry coupled to the output driver circuitry,
4 wherein:

5 in response to a first transition of the external clock
6 signal, the multiplexer circuitry couples the first portion of
7 data to an input of the output driver circuitry; and

8 in response to a second transition of the external clock
9 signal, the multiplexer circuitry couples the second portion
10 of data to the input of the output driver circuitry.

1 ¹⁵~~165~~. The system of claim ¹¹~~161~~ wherein both the rising edge
2 transition of the external clock signal and the falling edge
3 transition of the external clock signal transpire during a first
4 clock cycle of the external clock signal.

5 ¹⁶~~166~~. The system of claim ¹¹~~161~~ wherein both the rising and
6 falling edge transitions of the external clock signal include
7 voltage swings of less than one volt.

8 ¹⁷~~167~~. The system of claim ¹¹~~161~~ wherein the second integrated
9 circuit further includes a clock alignment circuit to receive the
10 external clock signal and to generate an internal clock signal,
11 wherein the input receiver circuitry on the second integrated
12 circuit device samples data in response to the internal clock
13 signal.

1 168. An integrated circuit device comprising:
2 output driver circuitry to output data onto a first external
3 signal line wherein:

4 the output driver circuitry outputs a first portion of
5 data in response to a rising edge transition of a first
6 external clock signal and the output driver circuitry outputs
7 a second portion of data in response to a falling edge
8 transition of the first external clock signal.

19 169. The integrated circuit device of claim 18 further
including input receiver circuitry to sample data from a second
external signal line wherein:

the input receiver circuitry samples a first portion
of data in response to a rising edge transition of a
second external clock signal; and

the input receiver circuitry samples a second portion
of data in response to a falling edge transition of the
second external clock signal.

20 170. The integrated circuit device of claim 19 further including
a clock alignment circuit to generate a first internal clock
signal, and wherein the input receiver circuitry samples the first
portion of data in response to the first internal clock signal.

1 ~~171.~~ The ~~system~~^{ci} of claim ~~170~~ wherein the clock alignment
2 circuit generates a second internal clock signal, and the input
3 receiver samples the second portion of data in response to the
4 second internal clock signal.

1 ~~172. The integrated circuit device of claim 168 wherein the~~
2 ~~clock alignment circuit generates an internal clock signal, and the~~
3 ~~output driver circuitry outputs data in response to the internal~~
4 ~~clock signal.~~

~~173~~. The integrated circuit device of claim ~~168~~ further including input receiver circuitry to sample data from the first external signal line wherein:

the input receiver circuitry samples a first portion of data in response to a rising edge transition of the first external clock signal; and

the input receiver circuitry samples a second portion of data in response to a falling edge transition of the first external clock signal.

~~174~~. The integrated circuit device of claim ~~168~~ further including:

multiplexer circuitry coupled to the ⁸output driver circuitry,
 wherein:

5 in response to a first transition of the first
6 external clock signal, the multiplexer circuitry couples the
7 first portion of data to an input of the ^{first} output driver
8 circuitry; and

9 in response to a second transition of the first
10 external clock signal, the multiplexer circuitry couples the
11 second portion of data to the input of the ^{first} output driver
12 circuitry.

25
1 175. The integrated circuit device of claim ²⁴ 174 further
including a clock alignment circuit to generate a first internal
clock signal using the first external clock signal, wherein the
multiplexer circuitry couples the first portion of data to the
input of the ^{first} output driver circuitry in response to the first
internal clock signal.

26
2 176. The integrated circuit device of claim ²⁵ 175 wherein the
clock alignment circuit generates a second internal clock signal,
3 and wherein the multiplexer circuitry couples the second portion of
4 data to the input of the ^{first} output driver circuitry in response to the
5 second internal clock signal.

1 177. The integrated circuit device of claim 176 further
2 including a clock alignment circuit coupled to the first external